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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/592,207	06/13/2000	Padma S. Nagarasa	00325.00355	7415

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EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2185	5

DATE MAILED: 09/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/592,207	NAGARASA ET AL.	
	Examiner	Art Unit	
	Albert Wang	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 15-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *27 June 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is responsive to Amendment A filed June 27, 2003. Claims 1-13 and 15-21 are pending.

Specification

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. The specification is objected to under 35 U.S.C. 112, first paragraph, as failing to support the subject matter set forth in the claims. The specification, as originally filed does not provide support for the invention as now claimed.

The test to be applied under the written description portion of 35 U.S.C. 112, first paragraph, is whether the disclosure of the application as originally filed reasonably conveys to the artisan that the inventor had possession at that time of later claimed subject matter. Vas-Cat, Inc. v. Mahurkar, 935 F. 2d 1555, 1565, 19 USPQ2d 111, 1118 (Fed. Cir. 1991), reh'rg denied (Fed. Cir. July 8, 1991) and reh'rg, en banc, denied (Fed. Cir. July 29, 1991).

The amended claims include the limitation "--- each of said plurality of delay times is less than a period of said clock signal ---". However, the specification does not provide an enabling disclosure to support this claimed limitation.

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it

pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-13 and 15-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In particular, claims 1-13 and 15-21 are rejected under 35 U.S.C. 112, first paragraph, for the reasons set forth in the objection to the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1, 2, 11-13 and 21 are rejected under 35 U.S.C. 102(a) as being anticipated by Dallas Semiconductor Datasheet, "DS1020 Programmable 8-Bit Silicon Delay Line", November 17, 1999 (hereinafter "DalSemi").

As per claim 1, DalSemi discloses an apparatus comprising:

a first circuit configured to

(i) receive a data signal (Fig. 1, IN) having a first setup/hold window with respect to a clock signal (Fig. 1, Clock (C)) and

(ii) present a delayed data signal (Fig. 1, OUT) having a second setup/hold window with respect to said clock signal, wherein

(i) a difference between said first setup/hold window and said second setup/hold window is configured in response to one or more of a plurality of delay times (Fig. 1, Programmable Delay),

(ii) each of said plurality of delay times is less than a period of said clock signal (Table 2 on page 4, maximum delay for DS1020-15 is 48.25 ns; AC Electrical Characteristics on page 6, minimum clock width is 50 ns) and

(iii) said plurality of delay times provides a user configurable delay (Fig. 1, via 8-bit input register) of said second setup/hold window relative to a transition of said clock signal.

As per claim 2, DalSemi further discloses a second circuit (Fig. 4, time interval counter) configured to receive said data delayed signal and present a data output.

As per claim 21, DalSemi discloses a total of all of said plurality of delay times is less than said period of said clock (Table 2 on page 4, maximum delay for DS1020-15 is 48.25 ns; AC Electrical Characteristics on page 6, minimum clock width is 50 ns).

As per claims 11-13, since DalSemi discloses the first delay circuit of claim 1, DalSemi discloses the claimed apparatus and method.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over DalSemi as applied to claims 1 and 12 above, and further in view of Brown, U.S. Patent No. 6,310,506.

As per claim 3, DalSemi as applied to claim 1 above does not expressly teach the details of said second circuit. Brown teaches a second circuit (Fig. 1B, input buffer 3 and latch 11), in conjunction with a first delayed circuit (delay network 5), comprising a register that is further configured in response to a clock signal (Fig. 1B, latch signal). DalSemi and Brown are analogous art because they are from the same field of endeavor involving programmable delay circuits. At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Brown's second circuit to DalSemi's apparatus in order to maintain the integrity of the apparatus.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over DalSemi as applied to claims 1 and 12 above, and further in view of JEDEC Standard No. 8-6, "High Speed Transceiver Logic (HSTL) - A 1.5 V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits", EIA/JESD8-6, August 1995 (hereinafter "JEDEC").

As per claim 4, while DalSemi teaches presenting a first signal in response to a data input, DalSemi does not expressly teach that said first delay circuit further comprises an HSTL circuit. HSTL is one of multiple transmission logic specifications in common use. It would have been a matter of design to have the first delayed circuit conform to the JEDEC standard. Therefore at the time of the invention, it would have been obvious to one of ordinary skill in the art to apply the JEDEC standard to DalSemi's apparatus.

7. Claims 5-10 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over DalSemi/JEDEC as applied to claims 4 and 12 above, and further in view of IBM Technical

Disclosure Bulletin, "Programmable Delay Line Control Signal Circuits", Vol. 37, No. 08, August 1994 (hereinafter "IBMTDB").

As per claim 5, DalSemi does not expressly teach the details of said first delay circuit. IBMTDB teaches a programmable delay line comprising multiple delay circuits (Figure, "series of seven delay elements"). DalSemi/JEDEC and IBMTDB are analogous art because they are from the same field of endeavor involving programmable delay circuits. At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply IBMTDB's programmable delay line to DalSemi/JEDEC's apparatus in order to maintain the integrity of the apparatus.

As per claim 6, IBMTDB teaches a switch (Figure, MUX).

As per claims 7 and 8, IBMTDB teaches a user configuration signal (Figure, via timing register) for selecting a delay which is for setup and hold timing.

As per claims 9 and 10, IBMTDB teaches said user configuration signal comprises a programmable multi-bit signal (Figure, 3-bit timing register).

As per claims 15-20, since DalSemi/JEDEC/IBMTDB teaches the apparatus of claims 4-10, the combination teaches the claimed method.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

aw
August 27, 2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100